L1CTT Status

- The entire L1CTT chain AFE → Mixer → DFEA → CTOC → CTTT for one or two Trigger Sectors functions as expected in the Combined Test Stand!

- L1CTT Tracks to L1Muon
  - L1CTT tracks were ~250 ns late for L1Muon to use in their trigger decisions. Over last couple of months a lot of work went into solving this issue.
  - Gained 6 RF ticks (~108 ns) by modifying DFEA and Mixer firmware. Confirmed by L1Muon.
  - Propagation of Global Reset to L1CTT digital boards implemented in AFEs and seen in DFEA. To be confirmed by L1Muon.
  - L1Muon was also able to cut down some of its time.
  - So, as things stand right now, with an additional 132 ns delay of the experiment's timing (i.e. TFW Level 1 decision time), L1CTT tracks should get to L1Muon *just* in time.
  - For various other reasons (discussed and decided upon in the dedicated Trigger Commissioning Meeting a couple of weeks ago) the plan is to in fact move TFW by 2 crossings, 2×132 ns.

L1CTT Status

- L1CTT Trigger Decisions (Terms) to TM/TFW
  - L1CTT chain functional in CTS. Moving to platform.
  - Working on understanding TFW inputs from L1CTT, not always in-sync, spurious control bits are suspect.
  - Start in the platform by propagating TVs from DFEA (and/or AFE) through the L1CTT chain to TM and TFW.
  - TVs implemented in DFEA firmware, easier to use than TVs in AFEs. DFEWare can easily turn on/off TS.
  - L1CTT overall latency estimated ~24–25 crossings. Need to measure *in situ* but expect to be in time, especially with the 2 additional crossings from TFW.
  - Raises the issue of L1 Pipeline depth in the L1CTT system. In most digital boards “easy” to go from 32- to 36-event deep pipeline implemented via on-chip DP RAMs. Or can go to the 396 ns mode, directly gaining a factor of ~2/3 in RAM memory.
- At present progress impaired by DFEA crate PS.
- Stability of trigger output of AFEs vital for operation of L1CTT, especially the SCL control bits and their sync.
- Discriminator output of AFEs under study.
- L1CTT communications to Level 2 & Level 3 via GLinks affected by clock jitter. Hardware solution in works. More on this from Steve/Stefan.